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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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08/801,812

02/14/1997

JOHN H. GIVENS

11675.106

6774

24247

7590

02/09/2007

TRASK BRITT

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EXAMINER

MALDONADO, JULIO J

ART UNIT

PAPER NUMBER

2823

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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3 MONTHS

02/09/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

**Office Action Summary**

Application No.

08/801,812

Applicant(s)

GIVENS, JOHN H.

Examiner

Julio J. Maldonado

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 20 November 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-6, 9-15 and 64 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6, 9-15 and 64 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

1. The addition of claim 64 as set forth in the in the response filed 11/20/2006 is acknowledged.
2. The rejection as set forth in the office action is withdrawn in view of the applicants' amendments.
3. Claims 1-6, 9-15 and 64 are pending in the application.

***Claim Rejections - 35 USC § 112***

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 1 recites, "...forming an electrically conductive layer on the seed layer over the top surface of the dielectric material and substantially within the recess such that voids are present within the recess...". Although there is support for the conductive layer covering the seed layer (Instant page 10, lines 7 – 14), there is no support in the submitted disclosure to the conductive layer substantially within the recess.

For purposes of this rejection the conductive layer is read as covering the seed layer as recited in the disclosure.

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-6, 9-15 and 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xu et al. (U.S. 5,847,461, hereinafter Xu '461) in view of Xu et al. (U.S. 6,217,721, hereinafter Xu '721) and Yim (U.S. 5,869,395).

Xu '461 (Figs.1-4) in a related method to form an interconnect teaches forming a recess (14) within a dielectric material (10) situated on a semiconductor substrate (2), wherein said recess (14) extends below a top surface (12) of said dielectric material (10); forming a diffusion barrier layer (20) comprising titanium nitride conformally on the top surface of the dielectric material (10) and over an interior surface of the recess (14); forming an electrically conductive layer (30) comprising aluminum on the barrier layer (20) and covering the top surface of the dielectric material (10), wherein the diffusion barrier layer (20) has a melting point greater than that of the electrically conductive layer (30); forming an energy absorbing layer (40) on said electrically conductive layer (30), wherein said energy absorbing layer (40) has a greater thermal absorption capacity than that of said electrically conductive layer (30) and wherein said energy absorbing layer (40) is selected from the group consisting of titanium, tungsten, silicon dioxide and

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tantalum; using a furnace to apply energy omnidirectionally to said energy absorbing layer (40) causing said electrically conductive layer (30) to flow within said recess (14); and patterning said interconnect (column 3, line 12 – column 7, line 45).

Xu '461 fails to disclose the steps of heating the diffusion barrier layer in an environment substantially containing nitrogen gas; forming a seed layer comprising titanium nitride on the diffusion barrier layer and over the dielectric material, wherein the diffusion barrier layer has a melting point greater than or equal to the seed layer; forming an electrically conductive layer on the seed layer including the portion of the seed layer within said recess, wherein the seed layer has a melting point greater than or equal to that of the electrically conductive layer.

However, Xu '721 (Fig.8) in a related method to form an interconnect teaches the steps of heating a diffusion barrier layer (162) in an environment substantially containing nitrogen gas; forming a seed layer (164) made of a graded titanium nitride, wherein said graded nitride starts as titanium nitride and ends as relatively pure titanium and is formed on a diffusion barrier layer (162) and over a dielectric material layer (142), wherein the diffusion barrier layer (162) has a melting point greater than or equal to that of the seed layer (164); and forming an electrically conductive layer (156) on the seed layer (164) including the portion of the seed layer (164) within a recess (152), wherein the seed layer (164) has a melting point greater than or equal to that of the electrically conductive layer (156) (column 3, line 65 – column 6, line 45).

Although Xu '461 teaches adverse effects that could happen by using a tungsten seed layer (Xu '461, column 1, line 63 – column 2, line 27), Xu '461 is silent on the use

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of other seed layers and thus is open to use the titanium nitride layer disclosed by Xu '721.

Also since said seed layer in Xu'721 is a composite of titanium nitride and titanium, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute titanium nitride layer 20 of Xu'461 with titanium nitride/titanium layer 164 of Xu'721, and use the titanium nitride part as a barrier layer and the titanium part as a seed layer, to arrive at the claimed invention. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a seed layer after the formation of the barrier layer and prior to the formation of the conductive layer, and having the thermal properties as taught by Xu '721 in the interconnect formation method of Xu '461, since heating the barrier layer in a nitrogen environment substantially reduces the electronic barrier at the metal-semiconductor interface (Xu '721, column 9, lines 39-45) and the addition of titanium nitride as a seed layer improves the flow of aluminum into an interconnect at moderate temperatures (Xu '721, column 6, lines 40-45).

Xu '461 in combination with Xu '721 substantially teach all aspects of the invention but fail to disclose that the diffusion barrier layer and the seed layer are deposited on the recess by a chemical vapor deposition process; that a chemical-mechanical polishing is used to remove portions of the energy absorbing layer and the electrically conductive layer; that the recess has an aspect ratio greater than about four to one; and that the recess comprises a contact hole situated below a trench, wherein said semiconductor substrate has a lower substrate and terminates at an opposite end

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thereof at said trench, and wherein said trench extends from said opposite end of said contact hole to a top surface of said dielectric material and parallel to the plane of the lower substrate.

However, Yim (Figs.2A-2K) in a related method to form an interconnect structure teaches the steps of depositing titanium nitride by a chemical vapor deposition process; using chemical-mechanical polishing to remove portions overlaying a damascene trench formed on a dielectric layer (210); providing a recess comprising a contact hole (260) situated below a trench (240); providing a semiconductor substrate (200) having a lower substrate (202) and terminating at an opposite end thereof at said trench (240), wherein said trench (240) extends from said opposite end of said contact hole (260) to a top surface of said dielectric material (210), and parallel to the plane of the lower substrate (202) (column 4, line 26 – column 7, line 31). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to deposit titanium nitride by chemical vapor deposition, using chemical mechanical polish to remove portions of conductive material overlying the dielectric layer and forming a recess comprising a trench and a contact hole as taught by Yim in the interconnect method of Xu '461 and Xu '721, since this would result in a damascene opening with an alignment tolerance, reduced processing time and a flat topography (Yim, column 3, line 49 – column 4, line 5).

Still, the combination of Xu '461 Xu '721 and Yim fail to disclose that the recess has an aspect ratio greater than about four to one. However, one of ordinary skill in the art at the time the invention was made would have been led to the claimed invention

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through routine experimentation to achieve desired device dimensions and therefore desired device density and desired device characteristics on the finished wafer. Also, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

### ***Conclusion***

8. Applicants are encouraged, where appropriate, to check Patent Application Information Retrieval (PAIR) (<http://portal.uspto.gov/external/portal/pair>) which provides applicants direct secure access to their own patent application status information, as well as to general patent information publicly available.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.



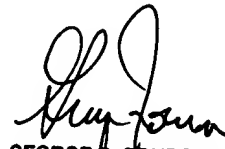
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10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax number for this group is 571-273-8300. Updates can be found at <http://www.uspto.gov/web/info/2800.htm>.



Julio J. Maldonado  
January 31, 2007

Julio J. Maldonado  
Patent Examiner  
Art Unit 2823



GEORGE R. FOURSON  
PRIMARY EXAMINER